

# MSFB1G, MSFB3G, MSFB5G, MSFB6G Bandwidth/Gain Selectable Bandpass Filter Data Sheet

## Description \_\_\_\_

The MSFBxG series of selectable filter ICs can be configured as 6 pole full, third or sixth octave response bandpass filter. The devices utilize low power and high precision Switched-Capacitor Filter (SCF) techniques that require only an external clock to set the corner frequencies for the lowpass filters. No external components (except for decoupling capacitors) are required.

The MSFB1G and MSFB3G are 50:1 clock to corner ratio bandpass filters for corner frequencies of up to 20 kHz and 3 kHz, respectively.

The MSFB5G and MSFB6G are 100:1 clock to corner ratio bandpass filters for corner frequencies of up to 20 kHz and 3 kHz, respectively.

Externally selectable gain setting pin and filter response select pin are included. The devices are packaged in a small 8-lead 4x4x0.9 mm VDFN package, making them very suitable for space constrained designs.

#### Absolute Maximum Ratings\_

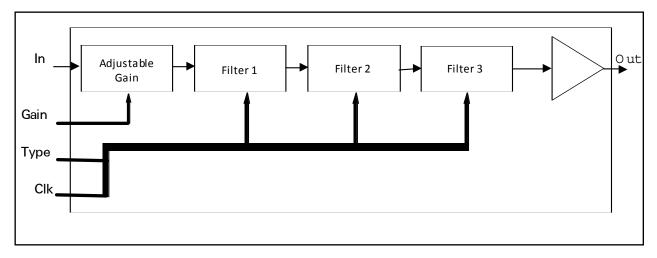
Power Supply Voltage	+6V
Storage Temperature Range	-60 <sup>0</sup> to +150 <sup>0</sup> C
Operating Temperature Range	-40 <sup>0</sup> to +85 <sup>0</sup> C

### Features

Low Voltage Operation down to 2.7V Three Distinct Filter Types in One Package Adjustable Gain Settings: 0, 10 or 20 dB No External Components High Precision Switched-Capacitor Filters Low Power Ideal for Battery Operated Applications Small Package Size

## Applications

Spectrum Analyzers General Purpose Telecom or Telephony Portable Systems Anti-Alias Filters Reconstruction Filters Tracking Filters Harmonic Analysis Noise Analysis Sensors and MEMS Distortion Analysis





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## Data Sheet

VDD=+3.0V, T=25°C, unless	otherwise	noted				
Parameter	Symbol	Min	Тур	Max	Units	Notes
DC Specifications						
Operating Voltage	VDD	2.7	3.0	5.5	V	
Supply Current	IDD		200	300	μΑ	MSFB3G/6G
			1	1.5	mA	MSFB1G/5G
Reference Voltage Output	VREF		1.5		V	
AC Specifications						
Gain Accuracy	GA	-0.5	0	0.5	dB	From selected value
Noise	<b>e</b> <sup>n</sup>		200		μVrms	To ½ sample
Distortion	THD		-72		dB	A weighted
Input Voltage	VINO			4	Vpp	Gain=0dB; VDD=5V
	V <sub>IN10</sub>			1.25	Vpp	Gain=10dB;VDD=5V
	V <sub>IN20</sub>			0.4	Vpp	Gain=20dB;VDD=5V
Input Impedance	Z <sub>IN</sub>		1		MΩ	f <sub>O</sub> =350 kHz
Output Voltage Range	Vout	0.5		4.5	V	
Output Drive	Ι <sub>Ο</sub>		300		μA	
Output Impedance	ZO		500		Ω	
Output Capacitive Load	C <sub>MAX</sub>			20	рF	
Clock to Center Ratio	CCR		50			MSFB1G/3G
			100			MSFB5G/6G
Center Frequency Range	CFR	0.0001		3	kHz	MSFB3G/6G
		0.0001		20	kHz	MSFB1G/5G
Ripple		,				i
Full Octave	R <sub>FO</sub>		0.2		dB	
Third Octave	<sup>R</sup> то		0.2		dB	
Sixth Octave	R <sub>SO</sub>		0.2		dB	
40 dB Bandwidth						
Full Octave	BWFO	0.3		3	Hz	Normalized Fo
Third Octave	BWTO	0.6		1.67	Hz	Normalized Fo
Sixth Octave	BWSO	0.76		1.32	Hz	Normalized Fo
Bandpass Q						1
Full Octave	Q		1.5			
Third Octave	Q		4.5		1	
Sixth Octave	Q		9			1

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# MSFB1G, MSFB3BG, MSFB5G, MSFB6G Bandwidth/Gain Selectable Bandpass Filter Data Sheet

Filter Selection Gain Selection The Gain control pin G is a tertiary control pin The filter type is selected using the filter select pin, TYPE. TYPE Is a tertiary control pin that where state 0 is GND, state 1 is VREF level selects the filter response. State 0 is GND, and state 2 is VDD. state 1 is VREF and state 2 is VDD. Gain G TYPE 0 OdB Bandpass 0 Full Octave 1 10dB 1 Third Octave 2 20dB 2 Sixth Octave The sample rate ratio is twice the clock to corner ratio (double sampling). Pin Description Pin Configuration OUT 1. Filter Output OUT TYPE 8 2 Filter Response Select Pin. IN 3. CLK CMOS Level Clock Input 4. G Gain Select Pin TYPE 2 7 VREF VDD 5. Positive Power Supply, Typically +1.5 Volts for Split Supply, +3.0 CLK 6 GND Volts for Single Supply Negative Power Supply, Typically 6 GND VDD GAIN 4 5 -1.5 Volts for Split Supply, O Volts for Single Supply 7. VREF Reference output, OV for Split Supplies +1.5 Volts Typical for Single Supply. For other VDD: Note that the large pads on the solder side of VREF = (VDD-VGND)/2the VDFN package is tied internally to VDD. Do 8`. IN Filter Input not ground this pad.

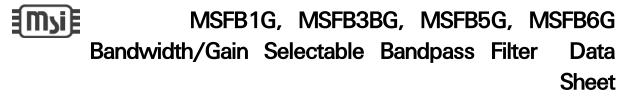
Ordering Information							
Part Number	Package	Clock to Corner Ratio	Max F				
MSFB1GD	8 Pin VDFN	50	20 kHz				
MSFB3GD	8 Pin VDFN	50	3 kHz				
		88	0 1112				
MSFB5GD	8 Pin VDFN	100	20 kHz				
MCERCOR		100	0.111-				
MSFB6GD	8 Pin VDFN	100	3 kHz				

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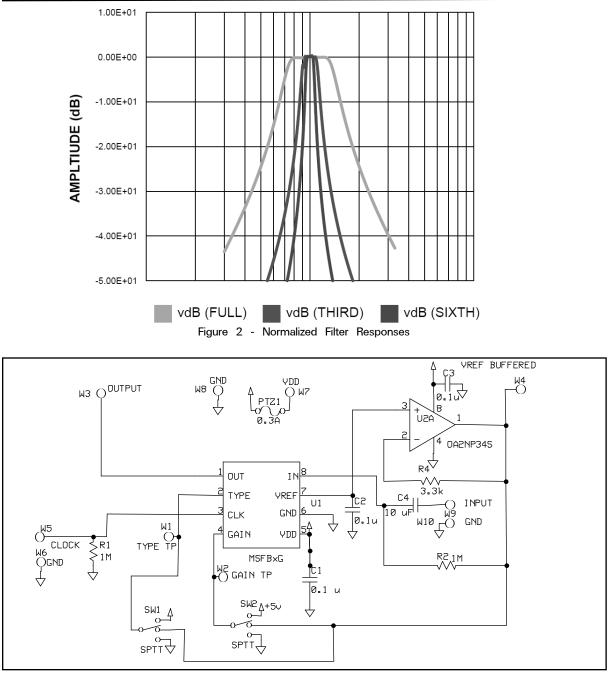


Figure 3 - Application Schematic

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